REFERENCE DOCUMENT FOR 300 PIN 40Gb TRANSPONDER

Description

This technical document has been created by the 300PIN MSA group. This document is offered to transponder users and suppliers as a basis for a technical agreement. However it is not a warranted document, each transponder supplier will have their own datasheet. If the user wishes to find a warranted document they should consult the datasheet of the chosen transponder supplier.

The MSA group reserves the rights at any time to add, amend or withdraw technical data contained in this document.

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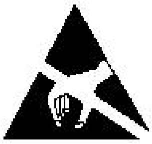
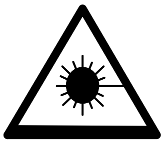
CAUTION : Components within the scope of this 40 Gbit/s TRANSPONDER MULTISOURCE are electrostatically sensitive and should not be handled except at a static free workstation. Invisible laser radiation, avoid direct exposure to beam.





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FIGURES LIST

Rev	Date	Originator(s)	Comment
1	March 5, 2002	Jeff Rollman	Creation
2	March 29,2002	Jeff Rollman	Incorporate changes made at Santa Clara MSA meeting
3	April 18, 2002	Jeff Rollman	Incorporate additional changes made at the Santa Clara MSA meeting
4	May 1, 2002	Jeff Rollman	Incorporate member changes
5	July 19, 2002	Jeff Rollman	Incorporate changes made at the Melbourne, FL MSA meeting.

Table 1: Modification History

REFERENCE DOCUMENTS

[1] Telcordia *GR-253* edition 3
[2] ITU-T *G.957*
[3] ITU-T *G.783*
[4] ITU-T *G.691*
[5] ITU-T *G.692*
[6] ITU-T *G.693*
[7] ITU-T *G.652*
[8] ITU-T *G.8251*
[9] OIF2001.145.X
[10] OIF2001.149.X
[11] IEEE *802.3ae Draft 2.3*

GLOSSARY

ITU-T	International Telecommunication Union - Telecommunication
SONET	Synchronous Optical Digital Network
SDH	Synchronous Digital Hierarchy
WDM	Wavelength Division Multiplexed
OIF	Optical Internetworking Forum
PRBS	Pseudo Random Binary Sequence

1.3 2km target distance application: 1310nm

1 OPTICAL CHARACTERISTICS

All min and max parameters are specified End-of-Life within the overall relevant operating case temperature range 0…+65°C unless otherwise stated.
The typical values are referenced to +25°C, nominal power supply, beginning of life.

Parameter	Cond.	Symb	Min	Typ	Max	Unit
ITU-T			VSR2000-3R1			
Target distance				2.0		km
Optical budget			0		4	dB
Dispersion					6.6	ps/nm
Center wavelength		λc	1290	1310	1330	nm
Transmitter						
Optical output power		S_{nom}	0		+3	dBm
Spectral width		$\Delta\lambda_{rms}$		TBD		nm
Extinction ratio		E_r	10			dB
SMSR			35			dB
Receiver						
Receiver sensitivity		R_{nom}	-5			dBm
Receiver overload		R_{nom}	+3			dBm
Path penalty					1	dB

Table 2: 2km application 1310nm

Optical tables are for reference purposes only. Latest Telcordia and ITU specifications should be consulted.

Parameter	Cond.	Symb	Min	Typ	Max	Unit
ITU-T			VSR2000-3R2			

1.5 25km target distance application : 1550nm

Target distance				2.0		km
Optical budget			0		4	dB
Dispersion					40	ps/nm
Center wavelength		λc	1530	1550	1565	nm
Transmitter						
Optical output power		S_{nom}	0		+3	dBm
Spectral width		$\Delta\lambda_{rms}$		TBD		nm
Extinction ratio		E_r	8.2			dB
SMSR			35			dB
Receiver						
Receiver sensitivity		R_{nom}	-5			dBm
Receiver overload		R_{nom}	+3			dBm
Path penalty					1	dB

Table 3: 2km application 1550nm

Optical tables are for reference purposes only. Latest Telcordia and ITU specifications should be consulted.

Parameter	Cond.	Symb	Min	Typ	Max	Unit
40Gb MSA				TBD		
Target distance				25		km
Optical budget			TBD		TBD	dB
Dispersion					TBD	ps/nm
Maximum DGD				TBD		ps
Center wavelength		λc	1530		1565	nm
Transmitter						
Optical output power		S_{nom}	-TBD		TBD	dBm
Spectral width		$\Delta\lambda_{rms}$		TBD		nm
Extinction ratio		E_r	TBD			dB
SMSR			35			
Receiver						
Receiver sensitivity		R_{nom}	TBD			dBm
Receiver overload		R_{nom}	TBD			dBm
Path penalty					TBD	dB

Table 4 : 25km target distance application : 1550nm

Optical tables are for reference purposes only. Latest Telcordia and ITU specifications should be consulted.

1.6 Long Haul : 1550nm

Parameter	Cond.	Symb	Min	Typ	Max	Unit
ITU-T			S-256.2			
Target distance				40		km
Optical budget			TBD		TBD	dB
Dispersion					TBD	ps/nm
Maximum DGD					TBD	ps
Center wavelength		λc	1530		1565	nm
Transmitter						
Optical output power		S_{nom}	TBD		TBD	dBm
Spectral width		$\Delta\lambda_{rms}$		TBD		nm
Extinction ratio		E_r	TBD			dB
SMSR			35			dB
Receiver						
Receiver sensitivity		R_{nom}	-TBD			dBm
Receiver overload		R_{nom}	TBD			dBm
Path penalty					TBD	dB

Table 5: Short Haul 1550nm

Optical tables are for reference purposes only. Latest Telcordia and ITU specifications should be consulted.

Parameter	Cond.	Symb	Min	Typ	Max	Unit
ITU-T			L-256.2			
Target distance				80		Km
Optical budget			TBD		TBD	dB
Dispersion					TBD	ps/nm
Maximum DGD				TBD		ps
Center wavelength		λc	1530		1565	nm
Transmitter						
Optical output power		S_{nom}	TBD		TBD	dBm
Spectral width		$\Delta\lambda_{rms}$		TBD		nm
Extinction ratio		E_r	TBD			dB
SMSR			35			dB
Receiver						
Receiver sensitivity		R_{nom}	TBD			dBm
Receiver overload		R_{nom}	TBD			dBm
Path penalty					TBD	dB

Table 6: Long Haul 1550nm

Optical tables are for reference purposes only. Latest Telcordia and ITU specifications should be consulted.

D-WDM application :
Can be covered by the Short-Haul/Intermediate-Reach and Long-Haul/Long-Reach spans. The definition of grid is based on the ITU-T grid from 1528.77 nm to 1563.86 nm with 100 GHz spacing (wavelength table will be added in future releases). L and S band are for further study.

1.7 Optical Measurement conditions
1.8 Jitter Characteristics

EXTINCTION RATIO MEASUREMENT CONDITIONS

Extinction ratio measurement should be per TIA OFSTP4A (Optical Fiber Standard Test Procedure). This requires testing with a fourth order Bessel-Thompson filter at the line rate with a PRBS of 2^{31}-1 data pattern.

1.7.1 Sensitivity measurement conditions

Sensitivity measurements should ideally be conducted with a BERT transmitter that matches the type of transmitter inside the Transponder module. Golden transmitters with high extinction ratios used for receiver sensitivity measurements can give misleading results if the device will receive a low extinction ratio transmitted signal when used in the field.

1.7.2 Eye mask measurement conditions

Transmitter module should pass OC768 SONET TX eye mask test per ITU-G.691 using PRBS pattern of 2^{23}-1 and 200 waveforms minimum.

Jitter transfer, generation, and tolerance should conform to GR-253, ITU-T G.783, ITU-T G.825.1 and IEEE 802.3ae Draft 2.3 specifications.
More detail on jitter measurement methods will be supplied in future revisions.

2 QUALIFICATION REFERENCE

Qualification requirements are TBD at this time.

3 ELECTRICAL CHARACTERISTICS

3.2 Electrical power supplies

All min and max parameters are specified End-of-Life within the overall relevant operating case temperature range 0…+65°C unless otherwise stated.
The typical values are referenced to +25°C, nominal power supply, beginning of life.
Customer must use the appropriate heat sink to make the case temperature within the recommended operating limits.

Parameters	Cond	Symb	Min	Typ	Max	Unit
+5V Analog Supply voltage		V_{+5VA}	4.75	5.0	5.25	V
+5V Analog Supply current		I_{+5VA}			1.35	A
+3.3V Analog Supply voltage		$V_{+3.3VA}$	3.13	3.3	3.47	V
+3.3V Analog Supply current		$I_{+3.3VA}$			2.7	A
+3.3V Digital Supply voltage		$V_{+3.3VD}$	3.13	3.3	3.47	V
+3.3V Digital Supply current		$I_{+3.3VD}$			3.6	A
-5.2V Analog Supply voltage		$V_{-5.2VA}$	- 5.45	- 5.2	- 4.94	V
-5.2V Analog Supply current		$I_{-5.2VA}$			2.7	A
-5.2V Digital Supply voltage		$V_{-5.2VD}$	- 5.45	- 5.2	- 4.94	V
-5.2V Digital Supply current		$I_{-5.2VD}$			3.15	A
APS Supply voltage	Note 1	V_{APS}	1.2		2.5	V
APS Supply current		I_{APS}			4.5	A
Power dissipation	Note 2			20	TBD	W
Ripple and Noise	Note 3				1%	mVpp

Note 1 – See Section 3.2.1 for a description of the adaptable power supply.

Note 2 – Power dissipation will be different for each module supplier depending on that vendors specific supply utilization.
Note 3 – Each voltage supply shall have less than 1% peak-to-peak ripple and noise from 1Hz to 20MHz under operating load conditions.
Note 4 – All voltages are measured at the connector interface.

Table 7: Power supply recommended operating limits

3.2.1 Adaptable Power Supply

The 40 Gb/s 300 pin MSA transponder will support an adaptable power supply (APS) on the APS supply voltage pins. The APS is capable of adjusting from a high of 2.5V to a low of 1.2V. The transponder shall support a voltage sense pin for the APS on the "APS Sense" pin (pin no. D13). This will be tied to the APS power supply rail inside the transponder. The transponder module shall also incorporate an "APS Set" pin (pin no. D17), with a resistor R1 between the APS set pin and ground (see figure X). Resistor values for R1 that are necessary to produce the required APS supply voltage are indicated in table X. If the host PCB does not wish to implement APS, then a fixed voltage can be supplied to the APS Supply pins while leaving APS Set and APS Sense open.

R2=470Ω, R3=1000 Ω

Resistor R1 (Ω)	Vout (V)

1530	1.2
672	1.5
330	1.8
0	2.5

Table 8: Resistor Values for R1

* It may be necessary to adjust these resistor values slightly to compensate for a voltage drop in the ground return path.

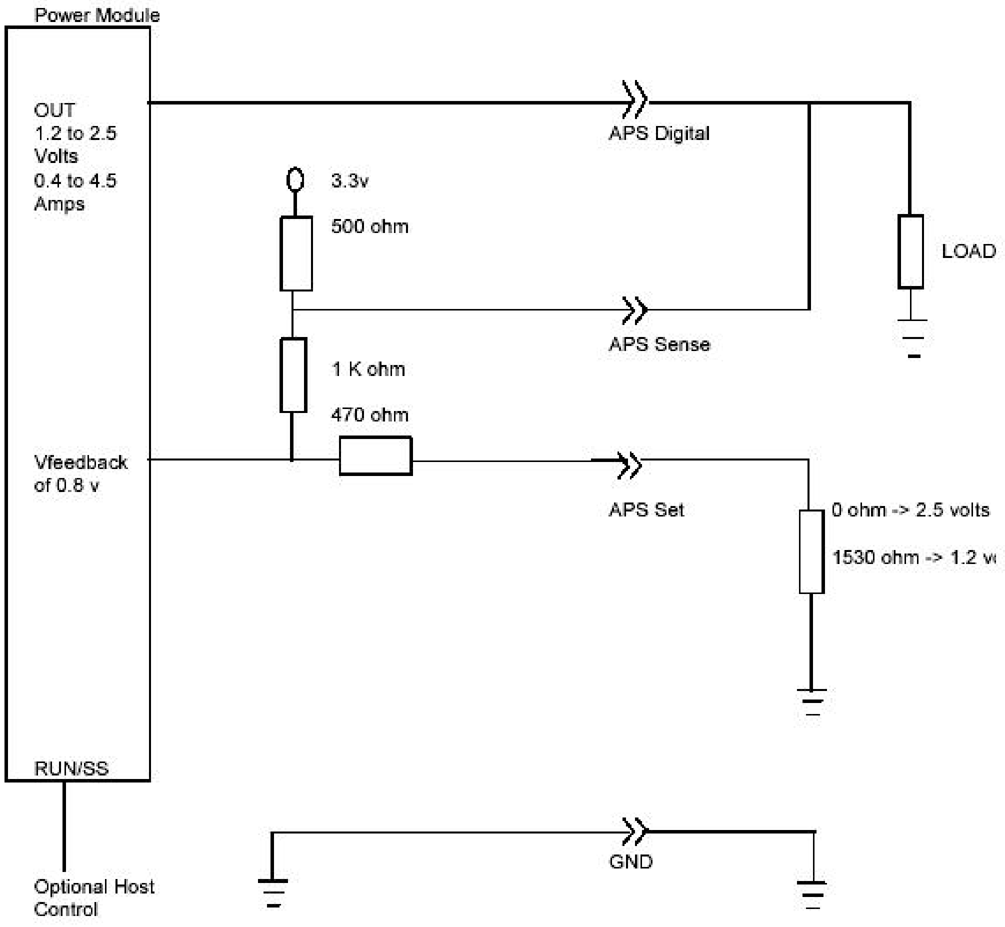


Figure 1: APS Conceptual Implementation

Adaptable Power Supply Reference

The APS supply on the host will regulate the APS voltage such that the voltage on the network labeled "Vfeedback" in Fig 1 becomes nominally 0.8 volts unless an APS voltage or current limiting condition takes priority. The resistors in Table 1 are calculated using resistors available as 1% values. For tolerance purposes, it is recommended that 0.1% resistors are used to provide additional tolerance margin although 1% may be suitable for some applications. These values are subject to change after a host back-plane is built and tested. Recommended tolerances are shown in Table 9.

Supply precision	1.5%

Supply load regulation	0.3%
Ground plane and ground connector drop	1.0%
Resistor tolerances using 0.1% parts	0.3%
Margin	0.9%
Total APS tolerance (+/-)	4.0%

Table 9: Recommended Tolerances (+/-)

3.2.2 Voltage calculation

The circuit shown in Fig 2 depicts one possible design that can be used to generate the APS voltage. Exact implementation and component values are not mandatory on the host. The APS implementer is responsible for ensuring that the transponder module is supplied in a manner which conforms to the APS tolerances stated in Table 3 for any given resistance between the module set pin and module ground.

Current capability of the APS

The APS will provide from 0.2 to 4.5 amperes and will current limit at typically 5 to 6 amperes.

Adaptable Power Supply Specs/Requirements

The host PCB will provide a steady state voltage on the adaptable voltage power conforming to the specifications given in Table 3.

APS steady state RMS ripple	<40mV rms
APS tolerance for a given resistance from	+/- 3%
APS set to ground.	
APS max overshoot after host power up	3% of V steady state
APS min rated current	0.4 Amps
APS maximum rated current for any voltage	4.5 Amps
APS current limit	5 ->6 Amps
TRANSPONDER total capacitance of	<200 uF
transceiver APS power pins	

Table 10: APS Tolerances (+/-)

3.2.3 Potential Licensing Issues

It should be noted that there is a possibility that part or all of the APS circuitry is covered by patents or patent applications owned by Agere. It is suggested that potential users of the APS contact Agere directly to determine the status of such patents.

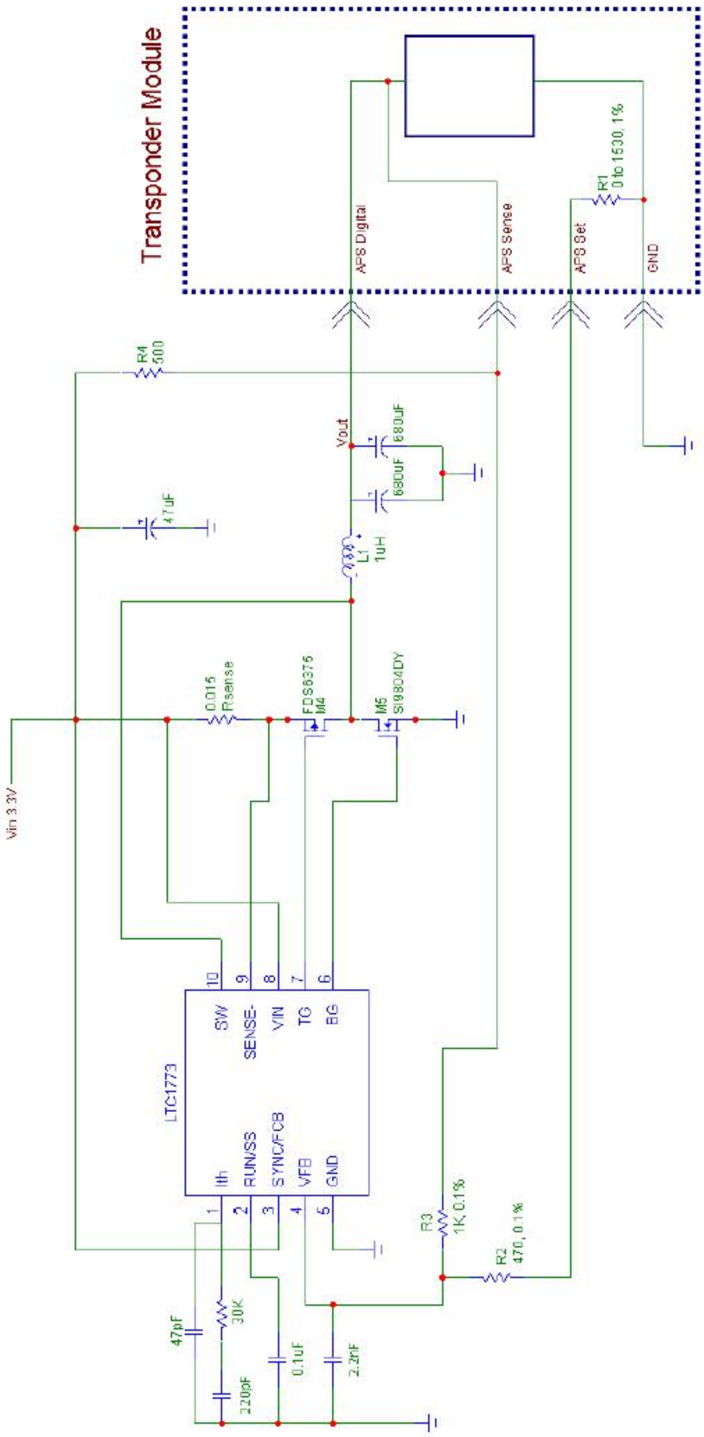
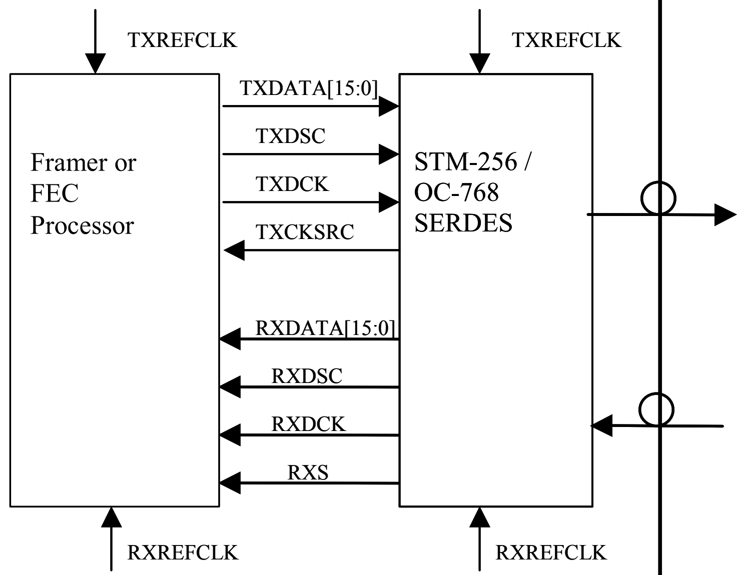


Figure 2: Example APS Implementation for 4.5A Supply

3.4 Electrical Input & output signals

The framer to SerDes Transceiver electrical interface should conform to guidelines outlined in Optical Internetworking Forum document OIF2001.145.x SFI-5:



Common electrical interface between framers and serializer/deserializer parts for OC-768/STM-256 interfaces.

Figure 3: Schematic Diagram of Framer or FEC processor to SerDes Transceiver Interface

All signals identified in Figure 3 are required to be sourced. The sink device (either the Framer/FEC Processor or the transponder manufacturer) must properly terminate all unused signals in a given application. Refer to OIF2001.145.x for a detailed description of the signals shown in Figure 1.

The SFI-5 data interface is defined to be a 1.2V CML as described in OIF2001.149.X. The transponder specified in this document will be both AC and DC compliant (drivers and receivers will support both AC and DC coupling). There will be no DC blocking capacitors on the transponder data lines. If AC coupling is required for operation, the customer is expected to implement the DC blocking capacitors on the line card.

3.4.1 LVCMOS Signal Characteristics

Unless otherwise specified, all digital control and alarm signals shall be 3.3V LVCMOS

Parameters	Cond	Symb	Min	Typ	Max	Unit
LVCMOS output high level			2 400		V_{DD1}	mV
LVCMOS output low level					400	mV
LVCMOS input high level			2 000		V_{DD1}	mV
LVCMOS input low level					800	mV

Table 11: LVCMOS Signal Characteristics

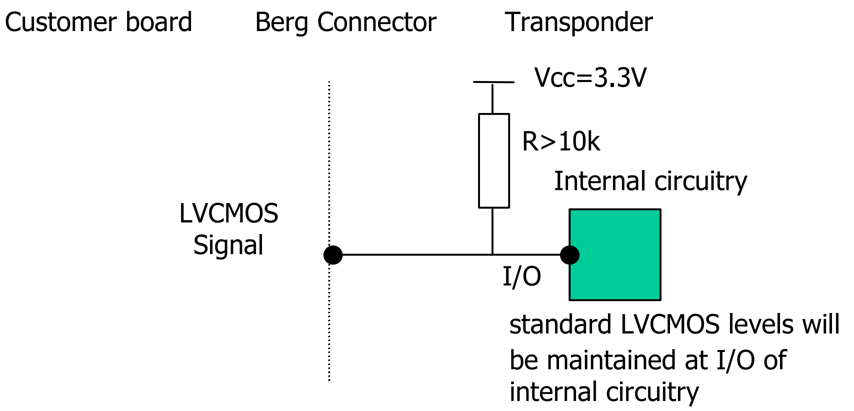


Figure 4: LVCMOS with pull-up resistor termination

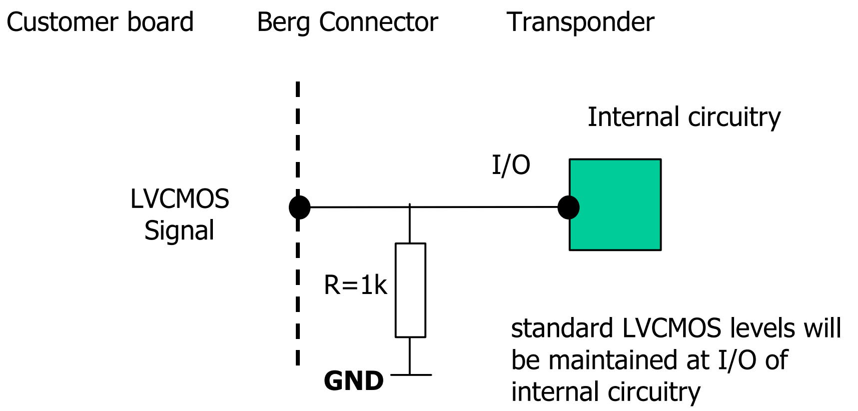


Figure 5: LVCMOS with pull-down resistor termination

3.4.2

3.4.3 Differential CML Input and Output Signals

Electrical characteristics of SFI-5 signals are defined in OIF2001.149.X. The tables in the following subsections are reproduced for convenience, but the referenced document should be consulted for actual requirements.

3.4.3.1 Differential Output Characteristics

All SXI-5 output drivers shall meet all the parameters in table 12.

Symbol	Parameter	Max	Min	Units	Comments
V_{CM}	Output Common Mode Voltage	1.23	0.72	V	$(V_{high} + V_{low}) / 2$. When using a load of Figure 5 with 1.05V<V_{tt}<1.35, 37.5<rterm<62.5 ohms, 0<Zvtt<30 ohms. Ground in Figure 5 is to be the same potential as the driver ground (see note 1). Parameter is unspecified if DC blocking capacitors are present.
T_{DRF}	Driver Rise/Fall Time		50	ps	At 20% - 80% into 100 ohm load
I_{DSHORT}	Short Circuit Current	100	-100	mA	To any voltage between 1.45 and –0.25 V, power on or off
UI_D	Unit Interval	402	372	ps	2.488 Gb/s to 2.689 Gb/s, ±100 ppm
R_{SE}	Single-ended output impedance	65	35	Ohm	at DC
R_D	Differential Impedance	125	75	Ohm	at DC
R_{HS}	Single-ended return loss		7.5	dB	From 0.004*baud rate to 0.75*baud rate
RL_{DIFF}	Differential return loss		7.5	dB	From 0.004*baud rate to 0.75*baud rate
V_{OH}	Differential output high level	V_{CM} + 0.5	V_{CM} + 0.17	V	Minimum value represents ¼ of the total loss allowed in the SxI-5 budget. See Figure 4 and Note 2.
V_{OL}	Differential output low level	V_{CM} - 0.17	V_{CM} - 0.5	V	Maximum value represents ¼ of the total loss allowed in the SxI-5 budget. See Figure 4 and Note 2.

Note 1: The Vtt values take into account the assumption of up to +/-50mV ground shift between drivers and receiver.

Note 2: In a DC coupled environment, these levels are a function of the received load illustrated in Figure 5. The maximum value will occur when V_{CM} is at the minimum level. The minimum value will occur when V_{CM} is at the maximum level.

Table 12: SxI-5 Differential Output Characteristics

3.4.3.2 Differential Input Characteristics

All SXI-5 input receivers shall meet all the parameters in table 13.

Symbol	Parameter	Max	Min	Units	Comments
V_{tt}	Termination Voltage	1.30	1.10	V	Parameter unspecified if DC blocking capacitors are present
V_{Rsense}	Input Sensitivity		.175	Vp-p	
Z_{Vtt}	Bias Voltage Source Impedance	30		Ohm	From DC to .75*baud rate if DC blocking capacitors are not present. From 500Mhz to .75*baud rate if DC blocking capacitors are present. (see note 1)
$T_{rise/fall}$	Rise/Fall time	0.36		UI	20-80%. Measured differentially into a 100 ohm load.
V_{Rmax}	Maximum Input Voltage	1.15		Vp-p	Zrterm=62.5 ohms. (See Figure 5) When Zrterm=50 ohms.
V_{RCM}	Input Common Mode Voltage	Vtt	0.7	V	$(V_{high} + V_{low}) / 2$ Parameter unspecified if DC blocking capacitors are present
Z_{INDIFF}	Differential input impedance	125	75	Ohm	At DC. If AC coupled, parameter applies at 0.0035 * Fdata only
L_{DR}	Differential return loss		10	dB	From 0.004*baud rate to 0.75*baud rate relative to 100 ohms
V_{IH}	Differential input high level	V_{RCM} + 0.5	V_{RCM} + 0.125	V	Minimum value represents ¼ of the total loss allowed in the SxI-5 budget. See Figure 4 and Note 2.
V_{IL}	Differential input low level	V_{RCM} - 0.125	V_{RCM} - 0.5	V	Maximum value represents ¼ of the total loss allowed in the SxI-5 budget. See Figure 4 and Note 2.

Note 1 : Magnitude of complex impedance with real part >0
Note 2 : In a DC coupled environment, these levels are a function of the received load illustrated in figure 5. The maximum value will occur when V_{CM} is at the minimum level. The minimum value will occur when V_{CM} is at the maximum level.

Table 13: SxI-5 Differential Input Characteristics

3.5 Analog Signals

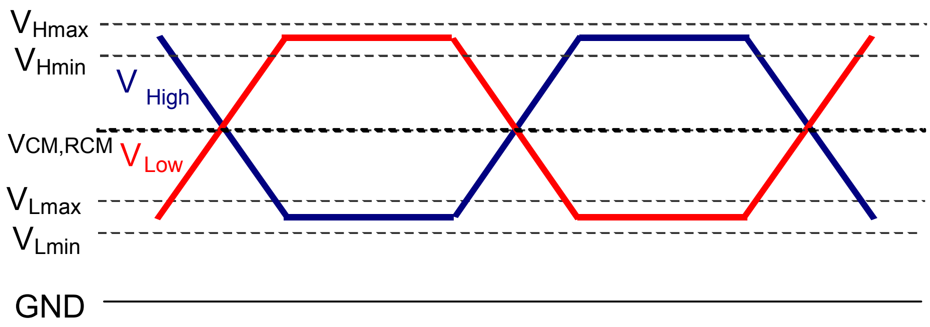


Figure 6: Common mode and differential mode definition; applies to both input and output signals

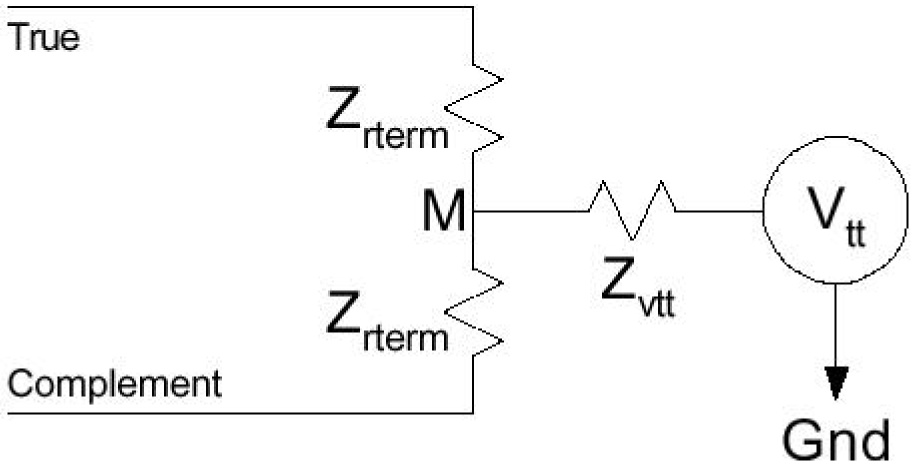


Figure 7: Termination and signaling

3.5.1 TXMONCK and RXMONCK

TXMONCK and RXMONCK are 50 ohm single ended clocks that can be used to monitor the transmit clock on the mux and receive clock on the demux. Acceptable frequencies are Fdata and Fdata/4. Preferably, the signal is derived from the CDR and CMU functions in the SERDES. These clocks are turned off during normal operation and startup. The I^2C interface will be used to enable the signals.

3.6 Clock Requirements

Parameters	Cond	Symb	Min	Typ	Max	Unit
TXMONCK Frequency		TXMON_Freq	$F_{data,min}$ or $F_{data,min}$ /4		$F_{data,max}$ or $F_{data,max}$ /4	MHz
TXMONCK Level		TXMON_LVL	200		450	mVpp
RXMONCK Frequency		RXMON_Freq	$F_{data,min}$ or $F_{data,min}$ /4		$F_{data,max}$ or $F_{data,max}$ /4	MHz
RXMONCK Level		RXMON_LVL	200		450	mVpp

Table 14: TXMONCK and RXMONCK Specifications

3.5.2 Threshold Adjust

The threshold adjust specifications and implementation characteristics are TBD at this time.

3.6.1 TXREFCK and RXREFCK

Parameters	Min	Typ	Max	Unit
TXREFCK Frequency	$F_{data,min}$ / 4		$F_{data,max}$ / 4	MHz
TXREFCK Jitter			1.8	ps (RMS)
TXREFCK Duty Cycle	45		55	%
TXREFCK Level	500		900	mV_{pp} (Single Ended)
TXREFCK Accuracy			30	ppm
RXREFCK Frequency	$F_{data,min}$ / 4		$F_{data,max}$ / 4	MHz
RXREFCK Jitter			1.8	ps (RMS)
RXREFCK Duty Cycle	45		55	%
RXREFCK Level	500		900	mV_{pp} (Single Ended)
RXREFCK Accuracy			30	ppm

Table 15: TXREFCK and RXREFCK Specifications

Figure 8 shows a block diagram of how TXREFCK and RXREFCK will be implemented in the module.

3.7 Alarms

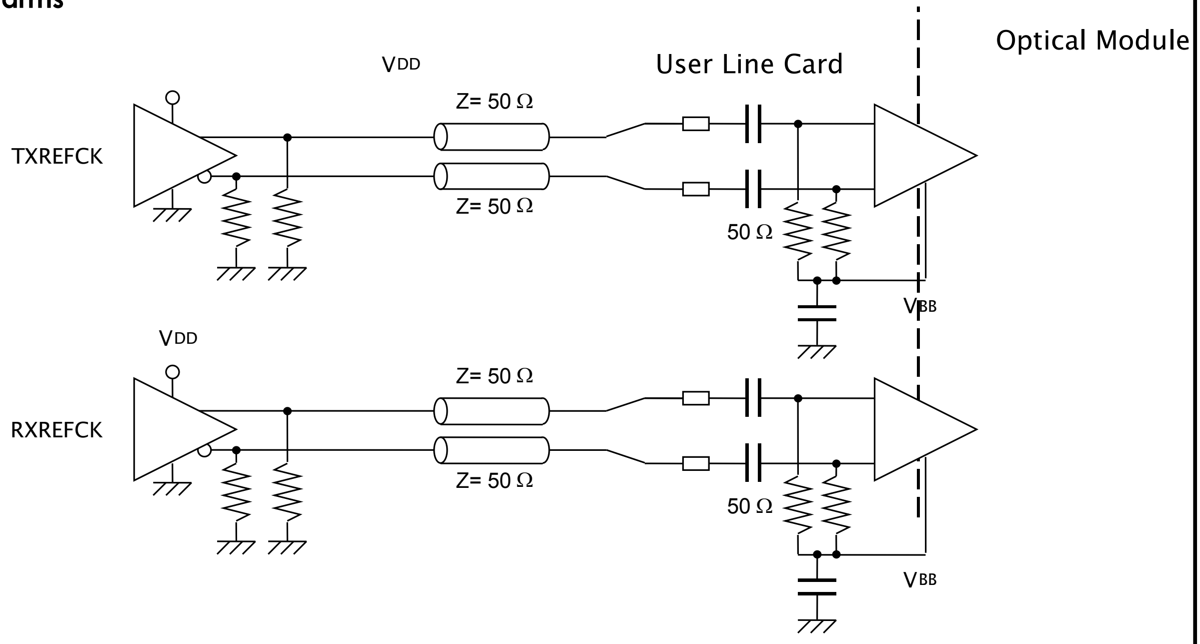


Figure 8: TXREFCK and RXREFCK Signal Implementation

3.7.1 Configurable Alarms response time

The alarms in Table 16 can be programmed for detection on the configurable alarm pin. All alarms are active low. Implementation of alarms in italics is not required by all module vendors.

Parameters	Cond	Symb	Min	Typ	Max	Unit
TX Laser bias current alarm activation time		LsBIASALM			10	ms
TX Laser bias current alarm deactivation time					10	ms
TX Laser temperature alarm activation time		LsTEMPALM			10	ms
TX Laser temperature alarm deactivation time					10	ms
TX Loss of lock of TXPLL activation time		TXLOCKERR			10	ms
TX Loss of lock of TXPLL deactivation time					10	ms
TX Mux FIFO error indicator activation time		*TXFIFOERR*			10	ms
TX Mux FIFO error indicator deactivation time					10	ms
TX Out of Alignment indicator activation time		TXOOA			10	ms
TX Out of Alignment indicator deactivation time					10	ms
RX Loss of DC power alarm activation time		*RXPOWALM*			10	ms
RX Loss of DC power alarm deactivation time					10	ms
PRBS error checker alarm activation time		*PRBSERRDET*			10	ms
PRBS error checker alarm deactivation time					10	ms
RX Loss of lock of RXDCK activation time		RXLOCKERR			10	ms
RX Loss of lock of RXDCK deactivation time					10	ms

Parameters	Cond	Symb	Min	Typ	Max	Unit
End of Life error indicator activation time		*EOL*			10	ms
End of Life error indicator deactivation time					10	ms
Power Supply Fault error indicator activation time		*PSUMMARY*			10	ms
Power Supple Fault error indicator deactivation time					10	ms

Table 16: Configurable Alarm Response Times

3.7.2 Hardware Alarms

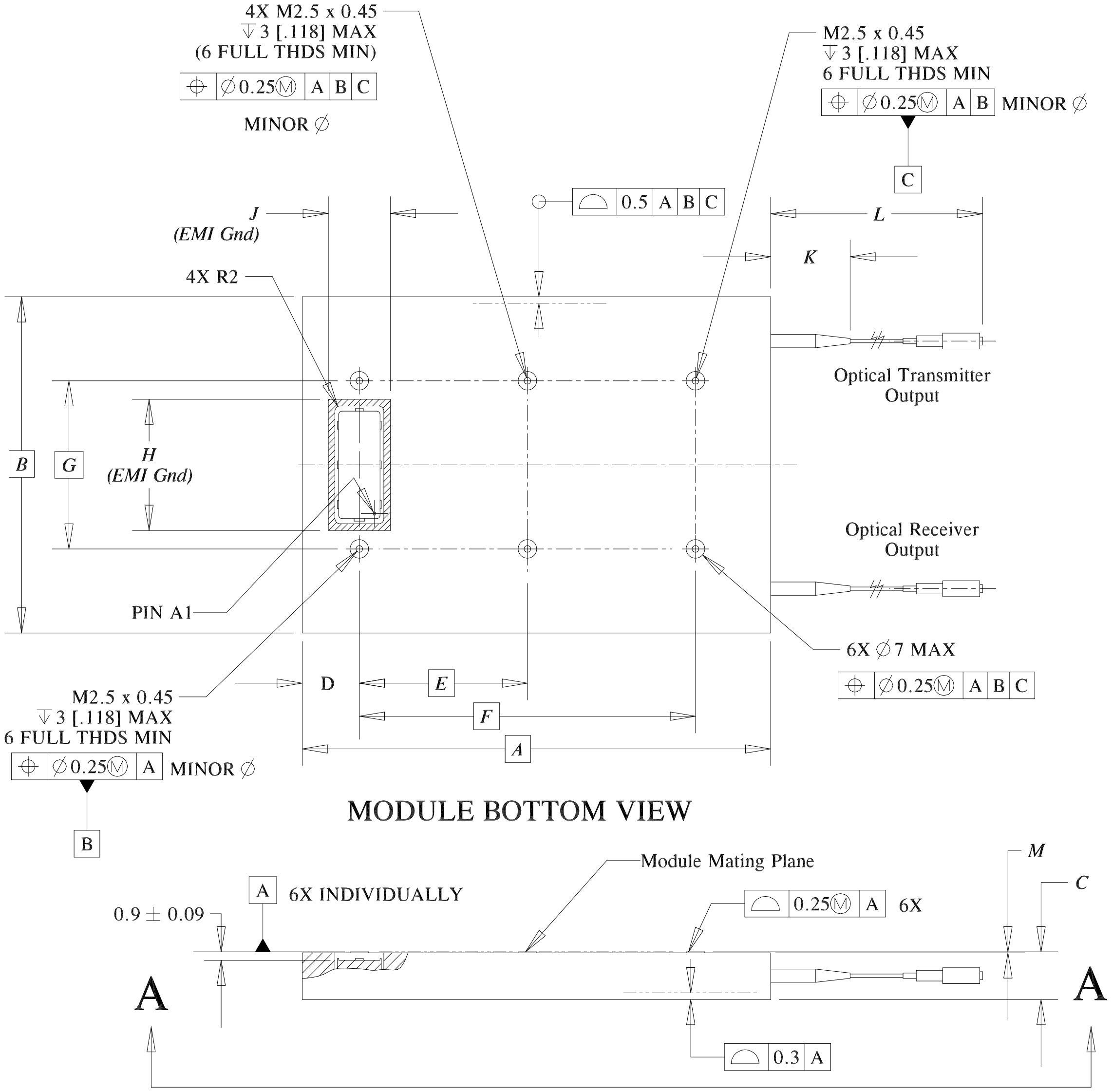
Parameters	Cond	Symb	Min	Typ	Max	Unit
Loss of RX Signal alarm activation time		*LOS*			10	ms
Loss of RX Signal alarm deactivation time					10	ms
Loss of RX Signal activation power			TBD		TBD	dBm
Loss of RX Signal deactivation power			TBD		TBD	dBm
Receive Status alarm activation time (note 1)		RXS			10	ms
Receive Status alarm deactivation time					10	ms

Note 1- RXS is defined by OIF2001.145.X.

Table 17: Hardware Alarm Response Times

4.1 Transceiver package drawing (from underneath to show electrical connector)

4 MECHANICAL DIMENSION



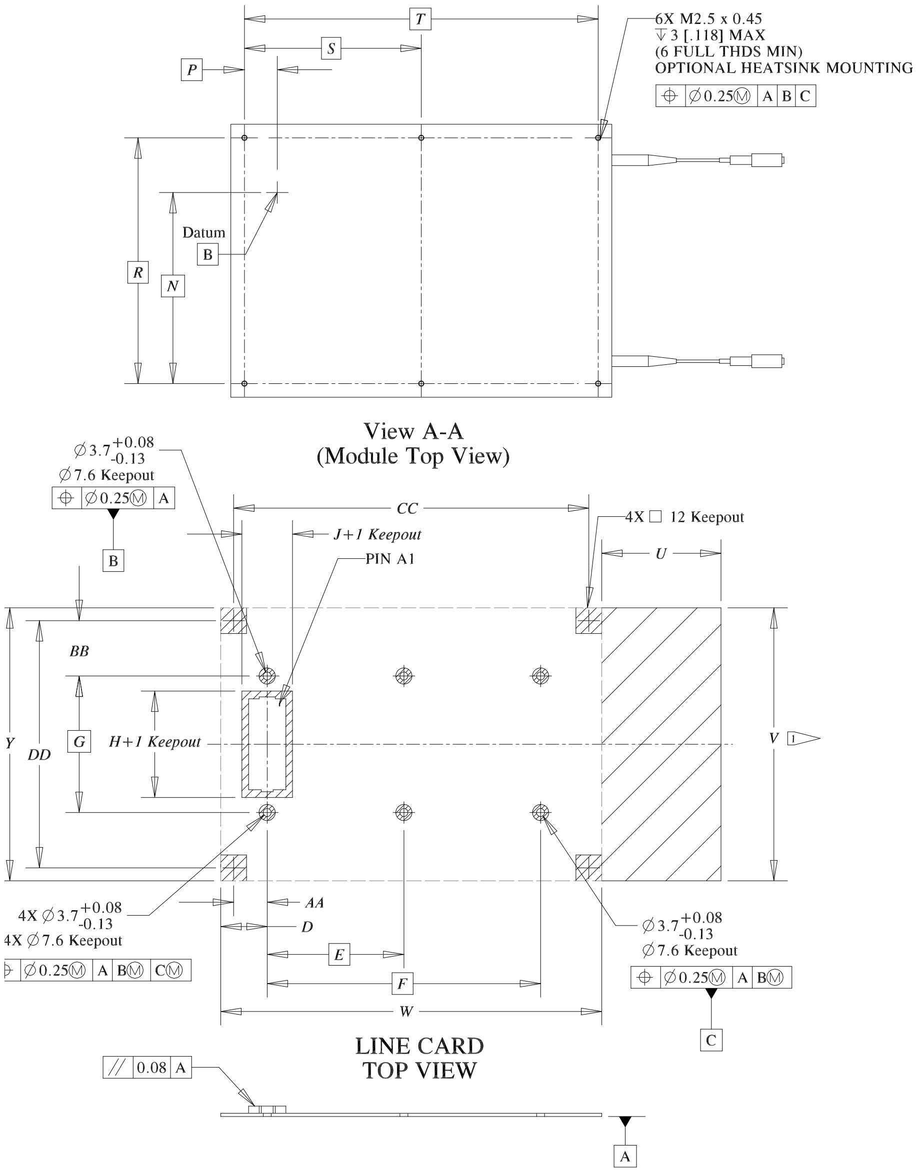


Figure 9: Transceiver package drawing

4.2 Connector description

Symbol	Minimum		Nominal		Maximum	
	Mm	[inch]	Mm	[inch]	Mm	[inch]
A					177	6.969
B					127	5.000
C					18	0.709
D			21.6	0.850		
E			63.5	2.500		
F			127	5.000		
G			63.5	2.500		
H			49.5	1.949		
J			23.5	0.925		
K					30	1.181
L	900	35.433	1000	39.370	1100	43.307
M					0.38	0.015
N			25.4	1.000		
P			15.25	0.600		
R			114.3	4.500		
S			82.15	3.234		
T			164.3	6.469		
U	55.4	2.181				
V	127	5.000				
W	177	6.969				
Y	127	5.000				
Z						
AA			15.6	0.614		
BB			25.75	1.014		
CC			165	6.496		
DD			115	4.528		

Table 18: 40 Gb/s Transponder Module Dimensions

FCI Meg-Array® 300 position receptacle, 1.27 mm x 1.27 mm (0.050 x 0.050 inch) ball to ball pitch, FCI part number 84501-10X. Mating line card connector shall be FCI part number 84500-002.

5 FIRMWARE INTERFACE WITH I²C BUS

The transponders are bi-directional optical/electrical converters that include serializer/deserializer functions. The interface is based on the MSA *I²C Reference Document For 300 Pin 10Gb and 40Gb Transponder*.

6.1 Top view from customer line card

6 PIN ASSIGNMENT

	K	J	H	G	F	E	D	C	B	A
1	Digital GND	RxDSCP	Digital GND	RxData12P	Digital GND	RxData8P	Digital GND	RxData4P	Digital GND	RxData0P
2	Digital GND	RxDSCN	Digital GND	RxData12N	Digital GND	RxData8N	Digital GND	RxData4N	Digital GND	RxData0N
3	*THRESH_ADJ*	Digital GND	-5.2V Digital	Digital GND	FFU	Digital GND	APS Digital	Digital GND	3.3V Digital	Digital GND
4	Digital GND	RxDCKP	Digital GND	RxData13P	Digital GND	RxData9P	Digital GND	RxData5P	Digital GND	RxData1P
5	Digital GND	RxDCKN	Digital GND	RxData13N	Digital GND	RxData9N	Digital GND	RxData5N	Digital GND	RxData1N
6	*LOS*	Digital GND	-5.2V Digital	Digital GND	I2C_ADDR_0	Digital GND	APS Digital	Digital GND	3.3V Digital	Digital GND
7	Digital GND	RxREFCKP	Digital GND	RxData14P	Digital GND	RxData10P	Digital GND	RxData6P	Digital GND	RxData2P
8	Digital GND	RxREFCKN	Digital GND	RxData14N	Digital GND	RxData10N	Digital GND	RxData6N	Digital GND	RxData2N
9	FFU	Digital GND	-5.2V Digital	Digital GND	I2C_ADDR_1	Digital GND	APS Digital	Digital GND	3.3V Digital	Digital GND
10	I2C_SDA	FFU	Digital GND	RxData15P	Digital GND	RxData11P	Digital GND	RxData7P	Digital GND	RxData3P
11	Digital GND	RxMONCK	Digital GND	RxData15N	Digital GND	RxData11N	Digital GND	RxData7N	Digital GND	RxData3N
12	I2C_SCL	Digital GND	RXS	Digital GND	I2C_ADDR_2	Digital GND	APS Digital	Digital GND	3.3V Digital	Digital GND
13	FFU	NUC	NUC	NUC	NUC	NUC	APS Sense	NUC	NUC	FFU
14	Analog Ground	-5.2V Analog	Analog Ground	-5.2V Analog	Analog Ground	3.3 V Analog	Analog Ground	3.3 V Analog	Analog Ground	5.0V Analog
15	Analog Ground	-5.2V Analog	Analog Ground	-5.2V Analog	Analog Ground	3.3 V Analog	Analog Ground	3.3 V Analog	Analog Ground	5.0V Analog
16	Analog Ground	-5.2V Analog	Analog Ground	-5.2V Analog	Analog Ground	3.3 V Analog	Analog Ground	3.3 V Analog	Analog Ground	5.0V Analog
17	FFU	NUC	NUC	NUC	NUC	NUC	APS Set	NUC	NUC	FFU
18	Digital GND	TxMONCK	FFU	FFU	Digital GND	FFU	FFU	FFU	FFU	FFU
19	LS_ENABLE	Digital GND	-5.2V Digital	Digital GND	CFG_ALM	Digital GND	APS Digital	Digital GND	3.3V Digital	Digital GND
20	Digital GND	TxDSCP	Digital GND	TxData12P	Digital GND	TxData8P	Digital GND	TxData4P	Digital GND	TxData0P
21	Digital GND	TxDSCN	Digital GND	TxData12N	Digital GND	TxData8N	Digital GND	TxData4N	Digital GND	TxData0N
22	STAT_INT	Digital GND	-5.2V Digital	Digital GND	*TxLINETIMSEL*	Digital GND	APS Digital	Digital GND	3.3V Digital	Digital GND
23	Digital GND	TxDCKP	Digital GND	TxData13P	Digital GND	TxData9P	Digital GND	TxData5P	Digital GND	TxData1P
24	Digital GND	TxDCKN	Digital GND	TxData13N	Digital GND	TxData9N	Digital GND	TxData5N	Digital GND	TxData1N
25	REG_RESET	Digital GND	-5.2V Digital	Digital GND	APS Digital	Digital GND	APS Digital	Digital GND	3.3V Digital	Digital GND
26	Digital GND	TxCKSRCP	Digital GND	TxData14P	Digital GND	TxData10P	Digital GND	TxData6P	Digital GND	TxData2P
27	Digital GND	TxCKSRCN	Digital GND	TxData14N	Digital GND	TxData10N	Digital GND	TxData6N	Digital GND	TxData2N
28	MOD_RESET	Digital GND	-5.2V Digital	Digital GND	APS Digital	Digital GND	APS Digital	Digital GND	3.3V Digital	Digital GND
29	Digital GND	TxREFCKP	Digital GND	TxData15P	Digital GND	TxData11P	Digital GND	TxData7P	Digital GND	TxData3P
30	Digital GND	TxREFCKN	Digital GND	TxData15N	Digital GND	TxData11N	Digital GND	TxData7N	Digital GND	TxData3N

Receiver

Transmitter

Differential Data / Clock Signals
Power Pins
Ground Pins
Control Signals

NUC: no user connection
FFU: reserved for future use
Italics:optional feature

Table 19: Top view from customer line card

6.2 Signal Definition

Electrical specifications for the SFI-5 interface can be found in OIF2001.145.X and OIF 2001.149.X. The signal descriptions for the SFI-5 bus are reproduced below.

Name	Type	I/O	Signal Description
TXDATA[15:0]	Diff CML Note 1	I	**Transmit Data Bus** SFI-5 compliant 16 wide transmit data bus from Framer/FEC chip.
TXDSC	Diff CML Note 1	I	**Transmit Deskew channel** used to deskew the TXDATA[15:0]
TXDCK	Diff CML Note 1	I	**Transmit Data Clock** provides a timing reference for transmit data. It is at ¼ data rate of TXDATA and TXDSC
TXREFCK	AC Coupled LVPECL Note 1	I	**Transmit Reference Clock** provides an alternate timing reference. The clock is at ¼ data rate of TXDATA and TXDSC
TXCKSRC	Diff CML Note 1	O	The **Transmit Reference Clock** (TXCKSRC) signal provides timing reference for the Transmit data path signals (TXDATA, TXDSC, TXDCK)
TXMONCK	Analog	O	**Transmit Monitor Clock** provides a single ended clock that can be used to monitor the transmit clock on the mux. This clock shall be turned off during normal operation and startup.
RXDATA[15:0]	Diff CML Note 1	O	**Receive Data Bus** SFI-5 compliant 16 wide receive data bus from SerDes
RXDSC	Diff CML Note 1	O	**Receive Deskew channel** used to deskew the RX_DATA[15:0]
RXDCK	Diff CML Note 1	O	**Receive Data Clock** provides a timing reference for receive data. It is at ¼ data rate of RXDATA and RXDSC
RXREFCK	AC Coupled LVPECL Note 1	I	**Receive Reference Clock** provides an alternate timing reference. The clock is at ¼ data rate of RXDATA and RXDSC
RXMONCK	Analog	O	**Receive Monitor Clock** provides a single ended clock that can be used to monitor the receive clock on the demux. This clock shall be turned off during normal operation and startup.
RXS	LV_CMOS Note 1	O	**Receiver Status** is an asynchronous signal used to indicate an alarm to the Framer (activehigh).
I2C_ADDR[2:0]	LV_TTL with 1k ohm pull down resistors Note 2	I	**I^{2}C Address[2:0]** is the 3 bit address provided to the transponder for the I^{2}C protocol. Each bit in the address shall be zero if left open.
I2C_SCL	Open Collector Note 2	I/O	**I^{2}C Clock** is a signal used to control the data transfer on the I^{2}C serial interface.
I2C_SDA	Open Collector Note 2	I/O	**I^{2}C Data** is a signal used to transfer data across the serial I^{2}C bus. The bus is used for control information and some alarms.

Name	Type	I/O	Signal Description
TXLINETIMSEL	*LVCMOS*	*I*	***Line Time Select*** *is used to select between source and line (loop) timing.*
LS_ENABLE	LVCMOS	I	**Laser Enable** is low to enable laser and driven high to disable laser. (internal pull-up in module)
LOS	*LVCMOS*	*O*	***Loss of Signal*** *is a signal to indicate to the there is no incoming optical signal (active low).*
THRESH_ADJ	*Analog*	*I*	***Threshold Adjust*** *is a signal used to control the receive signal threshold. This feature is shall be supported through I2C and not the THHRESH_ADJ pin.*
STAT_INT	LVCMOS	O	**Status Interrupt** is an electrical "or" of the status register (active low).
REG_RESET	LVCMOS	I	**Register Reset** is active low and when asserted to its low state will return all writable registers to their default state after resetting the CPU/CPLD on the transponder.
MOD_RESET	LVCMOS	I	**Module Reset** is active low and when asserted to its low state will reset the optical module. The module reset will force all components in the transponder to their reset state, including the I^2C registers, the laser and the respective chips.
CFG_ALM	LVCMOS	O	**User Configurable Alarm** is a user selectable alarm pin. TBD Alarm signals can be software configured to this pin.
APS Sense	Analog	O	**APS Sense** is a placeholder pin for the expected implementation of an APS (adjustable power supply) feature. When implemented, the 1.2V power supply lines will be converted to APS power supply lines. This will enable the SerDes chipset voltage to change for future designs.
APS_SET	Analog	0	**APS Set** is a placeholder pin for the expected implementation of an APS (adjustable power supply) feature. When implemented, the 1.2V power supply lines will be converted to APS power supply lines. This will enable the SerDes chipset voltage to change for future designs.

Note 1: These Signals are specified in SFI-5 OIF2001.145.x.
Note 2: See I2C document for clarification.

Table 20: Signal Definitions

6.3 Detailed pin description

6.3.1 "Row A" description

Pin #	Symbol	I/O	Logic	Description
A1	RxData0P	O	OIF SxI-5	Receiver Data Output
A2	RxData0N	O	OIF SxI-5	Receiver Data Output
A3	Digital GND	I	Supply	Digital Ground
A4	RxData1P	O	OIF SxI-5	Receiver Data Output
A5	RxData1N	O	OIF SxI-5	Receiver Data Output
A6	Digital GND	I	Supply	Digital Ground
A7	RxData2P	O	OIF SxI-5	Receiver Data Output
A8	RxData2N	O	OIF SxI-5	Receiver Data Output
A9	Digital GND	I	Supply	Digital Ground
A10	RxData3P	O	OIF SxI-5	Receiver Data Output
A11	RxData3N	O	OIF SxI-5	Receiver Data Output
A12	Digital GND	I	Supply	Digital Ground
A13	FFU	-	-	Reserved for Future Use
A14	5.0V Analog	I	Supply	Analog Power
A15	5.0V Analog	I	Supply	Analog Power
A16	5.0V Analog	I	Supply	Analog Power
A17	FFU	-	-	Reserved for Future Use
A18	FFU	-	-	Reserved for Future Use
A19	Digital GND	I	Supply	Digital Ground
A20	TxData0P	I	OIF SxI-5	Transmitter Data Input
A21	TxData0N	I	OIF SxI-5	Transmitter Data Input
A22	Digital GND	I	Supply	Digital Ground
A23	TxData1P	I	OIF SxI-5	Transmitter Data Input
A24	TxData1N	I	OIF SxI-5	Transmitter Data Input
A25	Digital GND	I	Supply	Digital Ground
A26	TxData2P	I	OIF SxI-5	Transmitter Data Input
A27	TxData2N	I	OIF SxI-5	Transmitter Data Input
A28	Digital GND	I	Supply	Digital Ground
A29	TxData3P	I	OIF SxI-5	Transmitter Data Input
A30	TxData3N	I	OIF SxI-5	Transmitter Data Input

Table 21: "Row A" Description

6.3.2 "Row B" description

Pin #	Symbol	I/O	Logic	Description
B1	Digital GND	I	Supply	Digital Ground
B2	Digital GND	I	Supply	Digital Ground
B3	3.3V Digital	I	Supply	Digital Power
B4	Digital GND	I	Supply	Digital Ground
B5	Digital GND	I	Supply	Digital Ground
B6	3.3V Digital	I	Supply	Digital Power
B7	Digital GND	I	Supply	Digital Ground
B8	Digital GND	I	Supply	Digital Ground
B9	3.3V Digital	I	Supply	Digital Power
B10	Digital GND	I	Supply	Digital Ground
B11	Digital GND	I	Supply	Digital Ground
B12	3.3V Digital	I	Supply	Digital Power
B13	NUC	-	-	No User Connect
B14	Analog Groun	I	Supply	Digital Ground
B15	Analog Groun	I	Supply	Digital Ground
B16	Analog Groun	I	Supply	Digital Ground
B17	NUC	-	-	No User Connect
B18	FFU	-	-	Reserved for Future Use
B19	3.3V Digital	I	Supply	Digital Power
B20	Digital GND	I	Supply	Digital Ground
B21	Digital GND	I	Supply	Digital Ground
B22	3.3V Digital	I	Supply	Digital Power
B23	Digital GND	I	Supply	Digital Ground
B24	Digital GND	I	Supply	Digital Ground
B25	3.3V Digital	I	Supply	Digital Power
B26	Digital GND	I	Supply	Digital Ground
B27	Digital GND	I	Supply	Digital Ground
B28	3.3V Digital	I	Supply	Digital Power
B29	Digital GND	I	Supply	Digital Ground
B30	Digital GND	I	Supply	Digital Ground

Table 22: "Row B" Description

6.3.3 "Row C" description

Pin #	Symbol	I/O	Logic	Description
C1	RxData4P	O	OIF SxI-5	Receiver Data Output
C2	RxData4N	O	OIF SxI-5	Receiver Data Output
C3	Digital GND	I	Supply	Digital Ground
C4	RxData5P	O	OIF SxI-5	Receiver Data Output
C5	RxData5N	O	OIF SxI-5	Receiver Data Output
C6	Digital GND	I	Supply	Digital Ground
C7	RxData6P	O	OIF SxI-5	Receiver Data Output
C8	RxData6N	O	OIF SxI-5	Receiver Data Output
C9	Digital GND	I	Supply	Digital Ground
C10	RxData7P	O	OIF SxI-5	Receiver Data Output
C11	RxData7N	O	OIF SxI-5	Receiver Data Output
C12	Digital GND	I	Supply	Digital Ground
C13	NUC	-	-	No User Connect
C14	3.3 V Analog	I	Supply	Analog Power
C15	3.3 V Analog	I	Supply	Analog Power
C16	3.3 V Analog	I	Supply	Analog Power
C17	NUC	-	-	No User Connect
C18	FFU	-	-	Reserved for Future Use
C19	Digital GND	I	Supply	Digital Ground
C20	TxData4P	I	OIF SxI-5	Transmitter Data Input
C21	TxData4N	I	OIF SxI-5	Transmitter Data Input
C22	Digital GND	I	Supply	Digital Ground
C23	TxData5P	I	OIF SxI-5	Transmitter Data Input
C24	TxData5N	I	OIF SxI-5	Transmitter Data Input
C25	Digital GND	I	Supply	Digital Ground
C26	TxData6P	I	OIF SxI-5	Transmitter Data Input
C27	TxData6N	I	OIF SxI-5	Transmitter Data Input
C28	Digital GND	I	Supply	Digital Ground
C29	TxData7P	I	OIF SxI-5	Transmitter Data Input
C30	TxData7N	I	OIF SxI-5	Transmitter Data Input

Table 23: "Row C" Description

6.3.4 "Row D" description

Pin #	Symbol	I/O	Logic	Description
D1	Digital GND	I	Supply	Digital Ground
D2	Digital GND	I	Supply	Digital Ground
D3	APS Digital	I	Supply	Digital Power
D4	Digital GND	I	Supply	Digital Ground
D5	Digital GND	I	Supply	Digital Ground
D6	APS Digital	I	Supply	Digital Power
D7	Digital GND	I	Supply	Digital Ground
D8	Digital GND	I	Supply	Digital Ground
D9	APS Digital	I	Supply	Digital Power
D10	Digital GND	I	Supply	Digital Ground
D11	Digital GND	I	Supply	Digital Ground
D12	APS Digital	I	Supply	Digital Power
D13	APS Sense	O	Supply	Sense Line for APS Supply
D14	Analog Groun	I	Supply	Analog Ground
D15	Analog Groun	I	Supply	Analog Ground
D16	Analog Groun	I	Supply	Analog Ground
D17	APS Set	-	-	Set Line for APS Supply
D18	FFU	-	-	For Future Use
D19	APS Digital	I	Supply	Digital Power
D20	Digital GND	I	Supply	Digital Ground
D21	Digital GND	I	Supply	Digital Ground
D22	APS Digital	I	Supply	Digital Power
D23	Digital GND	I	Supply	Digital Ground
D24	Digital GND	I	Supply	Digital Ground
D25	APS Digital	I	Supply	Digital Power
D26	Digital GND	I	Supply	Digital Ground
D27	Digital GND	I	Supply	Digital Ground
D28	APS Digital	I	Supply	Digital Power
D29	Digital GND	I	Supply	Digital Ground
D30	Digital GND	I	Supply	Digital Ground

Table 24: "Row D" Description

6.3.5 "Row E" description

Pin #	Symbol	I/O	Logic	Description
E1	RxData8P	O	OIF SxI-5	Receiver Data Output
E2	RxData8N	O	OIF SxI-5	Receiver Data Output
E3	Digital GND	I	Supply	Digital Ground
E4	RxData9P	O	OIF SxI-5	Receiver Data Output
E5	RxData9N	O	OIF SxI-5	Receiver Data Output
E6	Digital GND	I	Supply	Digital Ground
E7	RxData10P	O	OIF SxI-5	Receiver Data Output
E8	RxData10N	O	OIF SxI-5	Receiver Data Output
E9	Digital GND	I	Supply	Digital Ground
E10	RxData11P	O	OIF SxI-5	Receiver Data Output
E11	RxData11N	O	OIF SxI-5	Receiver Data Output
E12	Digital GND	I	Supply	Digital Ground
E13	NUC	-	-	No User Connect
E14	3.3 V Analog	I	Supply	Analog Power
E15	3.3 V Analog	I	Supply	Analog Power
E16	3.3 V Analog	I	Supply	Analog Power
E17	NUC	-	-	No User Connect
E18	FFU	-	-	Reserved for Future Use
E19	Digital GND	I	Supply	Digital Ground
E20	TxData8P	I	OIF SxI-5	Transmitter Data Input
E21	TxData8N	I	OIF SxI-5	Transmitter Data Input
E22	Digital GND	I	Supply	Digital Ground
E23	TxData9P	I	OIF SxI-5	Transmitter Data Input
E24	TxData9N	I	OIF SxI-5	Transmitter Data Input
E25	Digital GND	I	Supply	Digital Ground
E26	TxData10P	I	OIF SxI-5	Transmitter Data Input
E27	TxData10N	I	OIF SxI-5	Transmitter Data Input
E28	Digital GND	I	Supply	Digital Ground
E29	TxData11P	I	OIF SxI-5	Transmitter Data Input
E30	TxData11N	I	OIF SxI-5	Transmitter Data Input

Table 25: "Row E" Description

6.3.6 "Row F" description

Pin #	Symbol	I/O	Logic	Description
F1	Digital GND	I	Supply	Digital Ground
F2	Digital GND	I	Supply	Digital Ground
F3	FFU	-	-	For Future Use
F4	Digital GND	I	Supply	Digital Ground
F5	Digital GND	I	Supply	Digital Ground
F6	I2C_ADDR_0	I	LVTTL	Bit 0 of I2C Address Word (LSB)
F7	Digital GND	I	Supply	Digital Ground
F8	Digital GND	I	Supply	Digital Ground
F9	I2C_ADDR_1	I	LVTTL	Bit 1 of I2C Address Word
F10	Digital GND	I	Supply	Digital Ground
F11	Digital GND	I	Supply	Digital Ground
F12	I2C_ADDR_2	I	LVTTL	Bit 2 of I2C Address Word (MSB)
F13	NUC	-	-	No User Connect
F14	Analog Ground	I	Supply	Analog Ground
F15	Analog Ground	I	Supply	Analog Ground
F16	Analog Ground	I	Supply	Analog Ground
F17	NUC	-	-	No User Connect
F18	Digital GND	I	Supply	Digital Ground
F19	CFG_ALM	O	LVCMOS	User Configurable Alarm Pin
F20	Digital GND	I	Supply	Digital Ground
F21	Digital GND	I	Supply	Digital Ground
F22	*TxLINETIMSEL*	*I*	*LVCMOS*	*Tx Line Timing Select*
F23	Digital GND	I	Supply	Digital Ground
F24	Digital GND	I	Supply	Digital Ground
F25	APS Digital	I	Supply	Digital Power
F26	Digital GND	I	Supply	Digital Ground
F27	Digital GND	I	Supply	Digital Ground
F28	APS Digital	I	Supply	Digital Power
F29	Digital GND	I	Supply	Digital Ground
F30	Digital GND	I	Supply	Digital Ground

Table 26: "Row F" Description

6.3.7 "Row G" description

Pin #	Symbol	I/O	Logic	Description
G1	RxData12P	O	OIF SxI-5	Receiver Data Output
G2	RxData12N	O	OIF SxI-5	Receiver Data Output
G3	Digital GND	I	Supply	Digital Ground
G4	RxData13P	O	OIF SxI-5	Receiver Data Output
G5	RxData13N	O	OIF SxI-5	Receiver Data Output
G6	Digital GND	I	Supply	Digital Ground
G7	RxData14P	O	OIF SxI-5	Receiver Data Output
G8	RxData14N	O	OIF SxI-5	Receiver Data Output
G9	Digital GND	I	Supply	Digital Ground
G10	RxData15P	O	OIF SxI-5	Receiver Data Output
G11	RxData15N	O	OIF SxI-5	Receiver Data Output
G12	Digital GND	I	Supply	Digital Ground
G13	NUC	-	-	No User Connect
G14	-5.2V Analog	I	Supply	Analog Power
G15	-5.2V Analog	I	Supply	Analog Power
G16	-5.2V Analog	I	Supply	Analog Power
G17	NUC	-	-	No User Connect
G18	FFU	-	-	For Future Use
G19	Digital GND	I	Supply	Digital Ground
G20	TxData12P	I	OIF SxI-5	Transmitter Data Input
G21	TxData12N	I	OIF SxI-5	Transmitter Data Input
G22	Digital GND	I	Supply	Digital Ground
G23	TxData13P	I	OIF SxI-5	Transmitter Data Input
G24	TxData13N	I	OIF SxI-5	Transmitter Data Input
G25	Digital GND	I	Supply	Digital Ground
G26	TxData14P	I	OIF SxI-5	Transmitter Data Input
G27	TxData14N	I	OIF SxI-5	Transmitter Data Input
G28	Digital GND	I	Supply	Digital Ground
G29	TxData15P	I	OIF SxI-5	Transmitter Data Input
G30	TxData15N	I	OIF SxI-5	Transmitter Data Input

Table 27: "Row G" Description

6.3.8 "Row H" description

Pin #	Symbol	I/O	Logic	Description
H1	Digital GND	I	Supply	Digital Ground
H2	Digital GND	I	Supply	Digital Ground
H3	-5.2V Digital	I	Supply	Digital Power
H4	Digital GND	I	Supply	Digital Ground
H5	Digital GND	I	Supply	Digital Ground
H6	-5.2V Digital	I	Supply	Digital Power
H7	Digital GND	I	Supply	Digital Ground
H8	Digital GND	I	Supply	Digital Ground
H9	-5.2V Digital	I	Supply	Digital Power
H10	Digital GND	I	Supply	Digital Ground
H11	Digital GND	I	Supply	Digital Ground
H12	RXS	O	LVCMOS	Receiver Status Signal Output
H13	NUC	-	-	No User Connect
H14	Analog Ground	I	Supply	Analog Ground
H15	Analog Ground	I	Supply	Analog Ground
H16	Analog Ground	I	Supply	Analog Ground
H17	NUC	-	-	No User Connect
H18	FFU	-	-	Reserved for Future Use
H19	-5.2V Digital	I	Supply	Digital Power
H20	Digital GND	I	Supply	Digital Ground
H21	Digital GND	I	Supply	Digital Ground
H22	-5.2V Digital	I	Supply	Digital Power
H23	Digital GND	I	Supply	Digital Ground
H24	Digital GND	I	Supply	Digital Ground
H25	-5.2V Digital	I	Supply	Digital Power
H26	Digital GND	I	Supply	Digital Ground
H27	Digital GND	I	Supply	Digital Ground
H28	-5.2V Digital	I	Supply	Digital Power
H29	Digital GND	I	Supply	Digital Ground
H30	Digital GND	I	Supply	Digital Ground

Table 28: "Row H" Description

6.3.9 "Row J" description

Pin #	Symbol	I/O	Logic	Description
J1	RxDSCP	O	OIF SxI-5	Rx Deskew Channel
J2	RxDSCN	O	OIF SxI-5	Rx Deskew Channel
J3	Digital GND	I	Supply	Digital Ground
J4	RxDCKP	O	OIF SxI-5	Receiver Output Data Clock
J5	RxDCKN	O	OIF SxI-5	Receiver Output Data Clock
J6	Digital GND	I	Supply	Digital Ground
J7	RxREFCKP	I	LVPECL	Receiver 1/4 Rate Reference Clock
J8	RxREFCKN	I	LVPECL	Receiver 1/4 Rate Reference Clock
J9	Digital GND	I	Supply	Digital Ground
J10	FFU	-	-	Reserved for Future Use
J11	RxMONCK	O	Analog	1/4 or Full Rate Rx Clock Monitor
J12	Digital GND	I	Supply	Digital Ground
J13	NUC	-	-	No User Connect
J14	-5.2V Analog	I	Supply	Analog Power
J15	-5.2V Analog	I	Supply	Analog Power
J16	-5.2V Analog	I	Supply	Analog Power
J17	NUC	-	-	No User Connect
J18	TxMONCK	O	Analog	1/4 or Full Rate Tx Clock Monitor
J19	Digital GND	I	Supply	Digital Ground
J20	TxDSCP	O	OIF SxI-5	Tx Deskew Channel
J21	TxDSCN	O	OIF SxI-5	Tx Deskew Channel
J22	Digital GND	I	Supply	Digital Ground
J23	TxDCKP	I	OIF SxI-5	Transmitter Input Data Clock
J24	TxDCKN	I	OIF SxI-5	Transmitter Input Data Clock
J25	Digital GND	I	Supply	Digital Ground
J26	TxCKSRCP	O	OIF SxI-5	Transmitter 1/4 Rate Clock Source
J27	TxCKSRCN	O	OIF SxI-5	Transmitter 1/4 Rate Clock Source
J28	Digital GND	I	Supply	Digital Ground
J29	TxREFCKP	I	LVPECL	Transmitter 1/4 Rate Freq. Ref. Clock
J30	TxREFCKN	I	LVPECL	Transmitter 1/4 Rate Freq. Ref. Clock

Table 29: "Row J" Description

6.3.10 "Row K" description

Pin #	Symbol	I/O	Logic	Description
K1	Digital GND	I	Supply	Digital Ground
K2	Digital GND	I	Supply	Digital Ground
K3	*THRESH_ADJ*	*I*	*Analog*	*Receiver Threshold Adjust*
K4	Digital GND	I	Supply	Digital Ground
K5	Digital GND	I	Supply	Digital Ground
K6	*LOS*	*O*	*LVCMOS*	*Loss of Incoming Signal Alarm*
K7	Digital GND	I	Supply	Digital Ground
K8	Digital GND	I	Supply	Digital Ground
K9	FFU	-	-	Reserved for Future Use
K10	I2C_SDA	I/O	Open Collector	I2C Data Input/Output for Remote Access
K11	Digital GND	I	Supply	Digital Ground
K12	I2C_SCL	I	Open Collector	I2C Clock Input for Remote Access
K13	FFU	-	-	Reserved for Future Use
K14	Analog Groun	I	Supply	Analog Ground
K15	Analog Groun	I	Supply	Analog Ground
K16	Analog Groun	I	Supply	Analog Ground
K17	FFU	-	-	Reserved for Future Use
K18	Digital GND	I	Supply	Digital Ground
K19	LS_ENABLE	I	LVCMOS	Laser Enable Pin
K20	Digital GND	I	Supply	Digital Ground
K21	Digital GND	I	Supply	Digital Ground
K22	STAT_INT	O	LVCMOS	Electrical "OR" of the I2C Status Register
K23	Digital GND	I	Supply	Digital Ground
K24	Digital GND	I	Supply	Digital Ground
K25	REG_RESET	I	LVCMOS	Reset of all I2C Registers (active low)
K26	Digital GND	I	Supply	Digital Ground
K27	Digital GND	I	Supply	Digital Ground
K28	MOD_RESET	I	LVCMOS	Reset of all Module Components (active low)
K29	Digital GND	I	Supply	Digital Ground
K30	Digital GND	I	Supply	Digital Ground

Table 30: "Row K" Description

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